

# Michael Jones

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Expertise

## Hardware

Xilinx, Altera FPGA. Verilog synthesis & simulation. PCIe, NVMe, SAS, SATA, UFS and other serial protocols. DDR2. Board design. ATE architecture. Cadence, Synplicity, etc CAE. Rigorous specification, review, quality and source control standards.

## Software

Embedded NIOS. Mainly C. Some Python, C++, Perl. Basic HTML. Perforce, SVN, Clearcase. Windows. Linux. Office, Visio, Project, Visual Studio. Apache. Dreamweaver. CAE tool + license admin.

09/06 to present

ADVANTEST, San Jose, CA

## Senior Engineer

- Ultrascale+ design for Flash memory testing using PCIe protocols.
- Virtex-7 design for SSD module testing using SAS, SATA protocols.
- Virtex-6 design for Flash memory testing.
- Data bus design for Flash memory test instrument.
- Virtex-6/Stratix IV design for low power DDR2 memory testing.
- Developed from scratch an interface to a SerDes test module in Virtex-5.
- NIOS Embedded software design, coding and debug. RTL. Stratix II.
- Developed from scratch a histogram-generation FPGA for ADC testing in Virtex-4. Brought to production and wrote calibration and diagnostic programs in C++.
- Designed and developed group-wide simulation environment.
- Developed part of a Spartan-3E FPGA for measurement sequencing.

07/84 to 08/06

CREDENCE / NPTest / Schlumberger ATE, Milpitas, CA

## Senior Staff Engineer

Initially hired at Schlumberger as an Intern, was consistently promoted and given expanded responsibility to the Senior Staff level.

## Hardware experience includes:

- Designed and brought to production a 64bit/66MHz PCI card.
- Created ATE architectural design of major new product family.
- Designed hierarchical communication protocols (2MHz - 3GHz).
- Performed front-end design and layout analysis for 1.6GHz pin mux.
- Designed modules for a telecoms tester, incl. ISDN, T1/E1 and CDMA.
- Designed programmable PRBS and jitter generators for telecoms testing.
- Designed pin electronics, including use of thick film hybrid technology.
- Developed layout constraints and interfaced with layout engineers.

## FPGA experience includes:

- Developed and setup system simulation environment, including co-simulation from Python or target environment.
- Performed ionizing radiation reliability analysis (FPGA SEU).
- Acted as Internal consultant.
- Formulated FPGA design process and group website.
- Extensive use of Xilinx over 15 years. Over twenty designs covering families from the original XC2K to Virtex5 and most in between. More recent experience of Altera Stratix II and IV, including gigabit transceivers. Also some older families and Lattice devices.
- Implemented designs up to 300MHz system clock rate.
- Synthesized from Verilog using Quartus, Synplify Pro and Exemplar.

Professional  
Experience

07/84 to 08/06

CREDENCE / NPTest / Schlumberger ATE, Milpitas, CA

## Senior Staff Engineer (continued)

### Software experience includes:

- Embedded C.
- Wrote low-level diagnostics that enhanced testing. Mainly in C/C++.
- Wrote supporting scripts in various languages and OS's.
- Provided CAE tool administration and evaluation of new tools.
- Improved design team productivity by writing an internal static timing analysis tool which imported data from Cadence tools.
- Ported VxWorks to an embedded instrument processor.
- Implemented low level instrument drivers.
- Wrote system calibration programs for both timing and voltage.
- Wrote GUI for test equipment, running under X-Windows.

### Patents

- US 7043390. *Circuit Testing with Ring-Connected Test Instrument Modules.*
- US 7684280. *Histogram Generation With Banks For Improved Memory Access Performance.*
- US 8327090. *Histogram Generation With Mixed Binning Memory.*
- US 7831404. *Histogram Generation With Configurable Memory.*
- US 20150117130. *Programming multiple serial input devices.*
- US 9449714. *Flexible interrupt generation mechanism.*
- US 9239768. *Distributed pin map memory.*
- US 20160036684. *Both High Speed And Low Speed Signaling From The High Speed Transceivers On An Field Programmable Gate Array.*

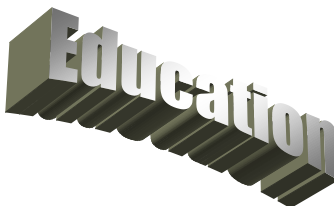
### Papers Published

- 2001 International Cadence User Group Conference. Author/presenter. *Ipi - A PCB-level static timing analysis tool.*
- 2004 International Test Conference, Author/presenter. *Digital Synchronization for Reconfigurable ATE*
- 2004 International Test Conference. Author. *System Monitor for Diagnostic, Calibration and System Configuration*

**B.Sc. (Hons.) Computer Science** - University of Manchester

### Training

Altera + Xilinx FPGA. Cadence + other CAE (including ConceptHDL, Spectraquest and Allegro). PCIe, NVMe, SAS, SATA, ISDN protocols. Verilog. Python. ASIC design. CDMA/spread-spectrum. Time Management. ATE programming. SEU analysis. TQM. Problem solving. Teamwork. Communication. Photoshop.



# Interests

## **Work Interests**

I enjoy jobs enabling me to combine my hardware and software skills for the same project. I enjoy variety, and especially FPGA design. I am particularly fussy about quality. I enjoy occasional travel, including international.

## **Nationality**

Dual US citizen and British citizen. Hold current passports from both.

## **Non-work Interests**

Folk dancing (Morris, Irish, English, International). Folk music. Folk song. Game playing (word, board, card). Photography. Cats. Ex-director of San Francisco Free Folk Festival. Irish community non-profit assistance.

*Carpe Diem*